High-Performance Ka-Band Monolithic Low-Noise Amplifiers Using 0.2-μm Dry-Recessed GaAs PHEMT's

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***Abstract*— Ka-band ultra-low-noise amplifiers fabricated with a manufacturable dry-recess process are presented. Low-damage selective dry etching was used for gate recess to achieve uniform threshold voltage (V_{th}) and saturation current (I_{dss}). Threefold improvement in V_{th} uniformity was achieved in comparison with the wet recess process. Fabricated PHEMT low-noise amplifiers (LNA's) employing 0.2-μm mushroom gates showed an average noise figure of 2.2 dB from 31–36 GHz with an associated gain of 22.5 dB. At the design frequency of 35 GHz, the noise figure was less than 2 dB. This is among the best results ever reported for Ka-band LNA's.**

I. Introduction

AlGaAs/InGaAs pseudomorphic HEMT (PHEMT) monolithic microwave integrated circuit (MMIC) technology has emerged as one of the key technologies for millimeter-wave applications. Excellent MMIC results have been demonstrated up to W-band with a relatively high level of integration [1]. Among various applications, PHEMT's are best suited to low-noise amplifiers (LNA's) due to their ultra-low-noise characteristics. Good noise figures with high gain have recently been demonstrated at Ka-band, which is the frequency range of this work. Two-stage LNA's for Ka-band receiver chips by Gamma Monolithics showed 2–3 dB noise figure with 12–14 dB gain from 30–34 GHz [2], and Hughes 0.25-μm PHEMT LNA's showed 3.5-dB noise figure with 15-dB associated gain at Ka-band [3]. InP-based HEMT's showed even lower noise figure and higher gain. An average noise figure of 2.3 dB with a 25-dB associated gain was achieved between 43 and 46 GHz using TRW 0.1-μm InP-based HEMT technology [4]. However, InP-based technology is less mature and reliability and manufacturability issues have not yet been addressed completely. On the other hand, GaAs PHEMT LNA's have proven reliability of an MTF of 2×10^6 h [5] and their process issues are much better understood. However, most of the mm-wave LNA's have so far been fabricated with wet gate recess process, which often resulted in nonuniformity of the threshold voltage (V_{th}) and the saturation current (I_{dss}). This problem can be solved with the use of selective dry recess [6]. In order to use the dry recess process for mm-wave LNA's, plasma damage during the gate recess must be low enough not to degrade the noise figure or the gain of the amplifier.

In this work, we present ultra-low-noise Ka-band PHEMT LNA's fabricated with a manufacturable 0.2-μm low-damage dry recess process. The three-stage LNA's showed an average noise figure of 2.2 dB with a 22.5-dB associated gain from 31–36 GHz.

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II. MMIC Fabrication and Circuit Design

The goal of this work was to develop ultra-low-noise amplifiers at Ka-band with a high yield and good uniformity. First of all, the gate length was selected to be 0.2 μm for this purpose; we determined that 0.2 μm was a good compromise between the yield and performance. Gates were defined using E-beam direct writing, and three-layer E-beam resists [PMMA/P(MMA-MAA)/PMMA] were employed to achieve clean lift-off and flag-free T-gates.

Another important feature of our process is the dry etch gate recess. Wet etch gate recess often resulted in considerable nonuniformity in I_{dss}'s and V_{th}'s. These nonuniformity problems could be somewhat alleviated by reducing the cap layer thickness, but at the expense of the source resistance. The source resistance is a crucial element in determining the noise figure, and the cap layer thickness could not be reduced below a certain level without affecting the source resistance and, thus, the noise figure. To achieve low noise figures and good uniformity at the same time, we have developed a low-damage selective dry etch recess process using BCl_3/SF_6 plasma. The RF power was about 20 W and the total etch time was less than 1 min. Under these conditions, the RF-induced dc bias was kept below -25 V, which ensured low damage. The etch selectivity between GaAs and $Al_{0.25}Ga_{0.75}As$ was higher than 100 : 1. The dry etch was followed by short wet etch to clean the etched surface and then by Ti/Pt/Au gate metal evaporation. The rest of the process included O_2 implant for device isolation, NiCr resistors, Si_3N_4 MIM capacitors, and air bridges. The devices were passivated with Si_3N_4 deposited by either PECVD or photo CVD (PCVD). After the front side process, the wafers were thinned to 75 μm and backside via holes were fabricated.

After the process, the devices were characterized by on-wafer dc, S-parameter, and noise parameter tests. Average

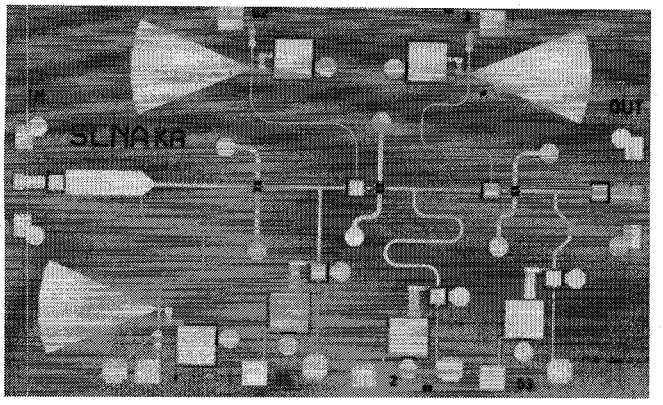

Fig. 1. Photograph of all source-feedback Ka-band monolithic LNA-SLNA (chip size = 2.5 mm × 1.5 mm).

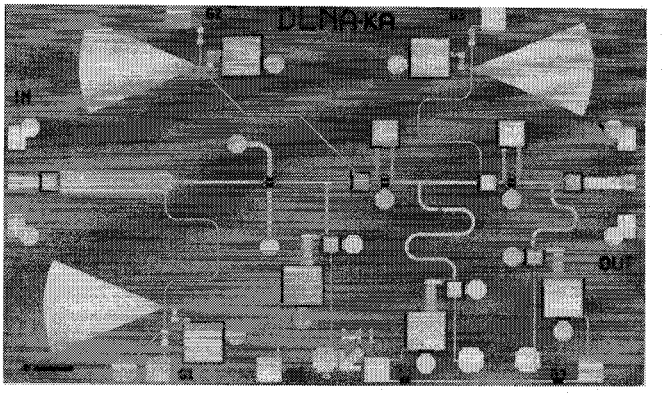

Fig. 2. Photograph of source/drain-feedback Ka-band monolithic LNA-DLNA(chip size = 2.5 mm × 1.5 mm).

threshold voltage (V_{th}) over 3-in wafers was −0.7 V. Typical V_{th} variation by this dry process was less than 7% (<50 mV), while that by the wet recess was 20% (<140 mV). Average f_T was 85 GHz and standard deviation was 3.5 GHz in 3-in wafers and 6 GHz in 4-in wafers. $f_{\max}$ was between 150–200 GHz depending on the bias. Typical measured $F_{\min}$ (minimum noise figure) at 18 GHz was about 0.7–0.8 dB with an associated gain of 12 dB. These values were slightly better or as good as the data obtained from the wet-etched devices, which demonstrates the low-damage nature of our dry recess process.

The circuit design goal was to build Ka-band amplifiers with a noise figure less than 2.5 dB and an associated gain higher than 22 dB. The LNA's were designed to operate between 32–36 GHz with a target frequency of 35 GHz. First, small-signal and noise models were obtained from multibias S-parameter measurements up to 40 GHz and noise parameter tests up to 18 GHz. Equivalent circuit parameters were extracted at each bias point from measured S-parameters using an analytical extraction method [7], [8]. Intrinsic noise elements were extracted by fitting the measured and modeled noise parameters. Based on these models, two three-stage circuits employing different feedback schemes were designed; one for lower noise figure and the other for higher gain. The first circuit, which was called "SLNA," used inductive feedback at the source terminal of all three-stage FET's. In this way, the optimum noise match and power match could be achieved simultaneously at each stage. The other circuit, which was called "DLNA," was designed for higher gain and used drain-to-gate parallel feedback in the second- and third-stage FET's. The first stage configuration was the same as in SLNA. Parallel RC feedback values were chosen to give DLNA 1–2 dB higher gain than SLNA. Negative feedback effect of the parallel feedback design was weaker than that of the series feedback, resulting in a slightly higher gain in DLNA. The simulated noise figure was also higher in DLNA by 0.2 dB. At each stage of both LNA's, a HEMT with four gate fingers 0.2 μm long and 20 μm wide was used.

The photographs of SLNA and DLNA are shown in Figs. 1 and 2, respectively. The chip size was 2.5 mm × 1.5 mm in both cases. No attempts were made in this first pass design to minimize the chip size.

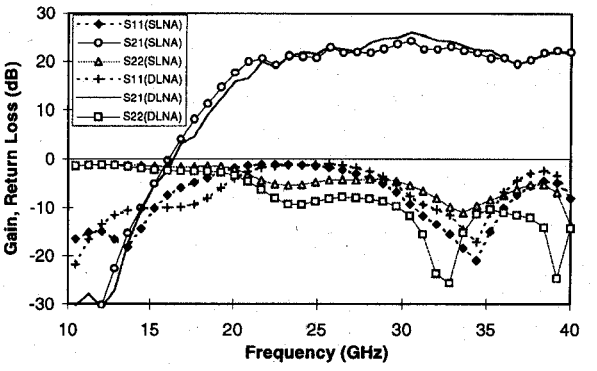

Fig. 3. Measured gain and input and output return loss of SLNA and DLNA.

III. Experimental Result

In order to measure gain bandwidth characteristics, the chips were first tested on wafer using HP 8510C network analyzer. For this measurement, the circuits were biased for maximum gain rather than for minimum noise figure. Measured gain and return loss of both SLNA and DLNA are shown in Fig. 3. As expected, DLNA showed about 1–2 dB higher gain than SLNA from 30–35 GHz. Output return loss was better in DLNA (−11 dB versus −8.5 dB at 35 GHz), while input return loss was better in SLNA (−18 dB versus −14 dB at 35 GHz). Both LNA's demonstrated ultra-broadband characteristics showing gains higher than 20 dB from 23–40 GHz.

The noise figure and associated gain were measured from 31–36 GHz. A preamplifier with more than 20 dB gain and less than 3-dB noise figure was used for the noise measurement. In this way, the uncertainty in the noise figure measurement could be reduced below 0.15 dB. Measured noise figure and gain of both LNA's under low-noise bias conditions are shown in Fig. 4. This result represents the data averaged over three wafers from two different lots. Both LNA's were tested under the same voltage bias conditions. The average noise figure from 31–36 GHz was 2.2 dB for SLNA and 2.5 dB for DLNA. The noise figure at 35 GHz was less than 2 dB (1.8 dB) for SLNA, which represents state-of-the-art noise figure data. The average associated gain for the same frequency range was 22.5 dB for SLNA and 24 dB for DLNA. The gain variation of SLNA from 31–36 GHz was about 2 dB, and the corresponding noise figure variation was less than 1 dB. Power characteristics of

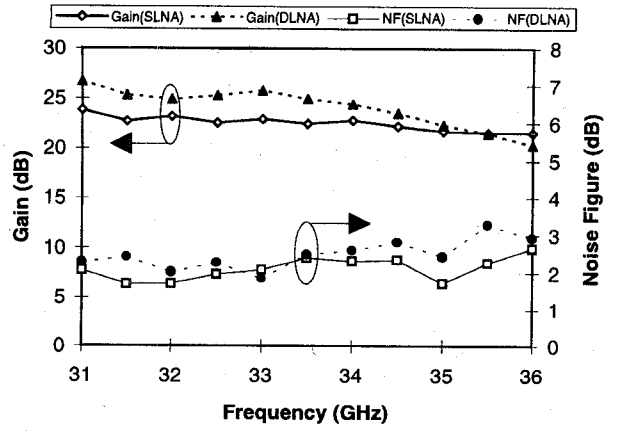

Fig. 4. Measured average noise figure and associated gain of SLNA and DLNA.

the LNA's were also measured. The saturation power was 12.5 dBm and 1-dB gain compression power was 10.5 dBm.

IV. Conclusion

In this work, we have developed ultra-low-noise Ka-band LNA's using 0.2-μm dry recess PHEMT technology. Low-damage dry etch gate recess yielded low noise figures and good uniformity. Threefold enhancement in V_{th} uniformity was achieved by dry recess process. Two types of LNA's were designed and fabricated. Both LNA's showed ultra broadband characteristics, demonstrating more than 20 dB gain from 23–40 GHz. The average noise figure of SLNA between 31–36 GHz was 2.2 dB with an associated gain of 22.5 dB, which was among the best results ever reported for Ka-band LNA's. At the design frequency of 35 GHz, the noise figure was less than 2 dB. These circuits are well-suited to high-volume and high-performance mm-wave front-end applications.

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